3A, 23V, Synchronous Step-Down DC/DC

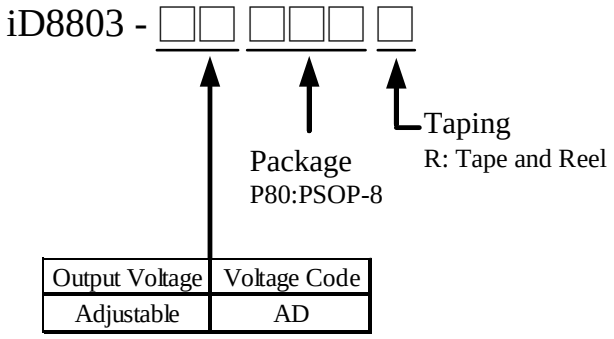
General Description

The iD8803 is a 340kHz fixed frequency PWM synchronous step-down regulator. The iD8803 is operated from 4.5V to 23V, the generated output is adjustable from 0.925V to 0.8Vin; and the continuous output current can be up to 3A.

The MOSFETs of 90mΩ on resistance are integrated in this device. The current mode control provides fast transient response and cycle-by-cycle current limit. The shutdown current is 0.3μA typical. Adjustable soft start prevents inrush current at turn on.

The iD8803 is with thermal shutdown. The iD8803 is available in the PSOP-8L package, and it is RoHS compliant and 100% lead (Pb) free.

Ordering Information



Applications

- Distributed power systems
- Networking systems
- FPGA, DSP, ASIC power supplies
- Notebook computers
- Green electronics or appliance

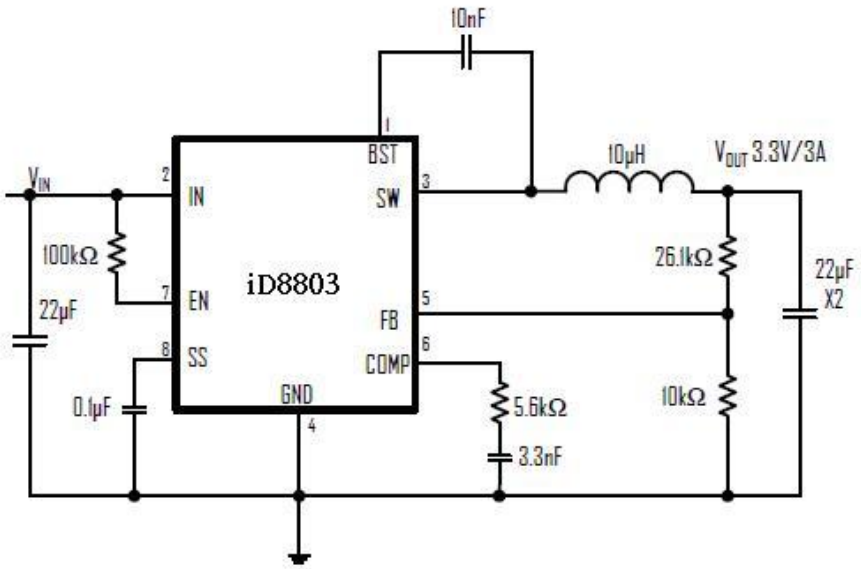
Features

- 4.5V to 23V input voltage
- Output adjustable from 0.925V to 18V
- Output current up to 3A
- Integrated 90mΩ power MOSFET switches
- UVLO protection
- Shutdown current 0.3μA typical
- Efficiency up to 96%
- 340kHz fixed frequency
- Programmable soft start
- Over current protection
- Over temperature protection
- RoHS Compliant and 100% Lead (Pb) Free

Marking Information

For marking information, please contact our sales representative directly or through distributor around your location.

Typical Application Circuit



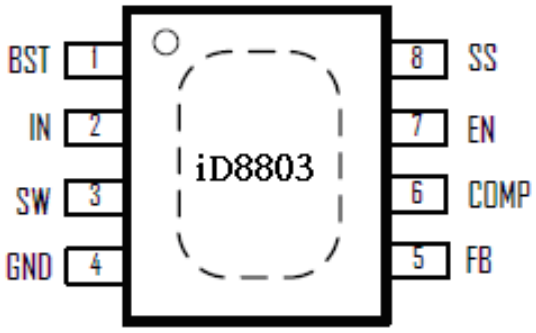
Absolute Maximum Ratings

Supply Voltage V_{IN}	–0.3V to +26V
Switch Node V_{SW}	–0.3V to V_{IN}+0.3V
Boost V_{BS}	V_{SW}–0.3V to V_{SW}+6V
Enable V_{EN}	–0.3V to V_{IN}+0.3V
All Other Pins	–0.3V to +6V
Power Dissipation, P_D @ T_A=25°C	
PSOP-8	1.33W
Thermal Resistance, θ_{ja}	
PSOP-8	75°C/W
Max. Junction Temperature	150°C
Storage Temperature	-65°C to 150°C

Recommended Operating Conditions

Input Voltage V_{IN}	4.5V to 23V
Junction Temperature	-20°C to 125°C
Ambient Operating Temperatures	-40°C to 85°C

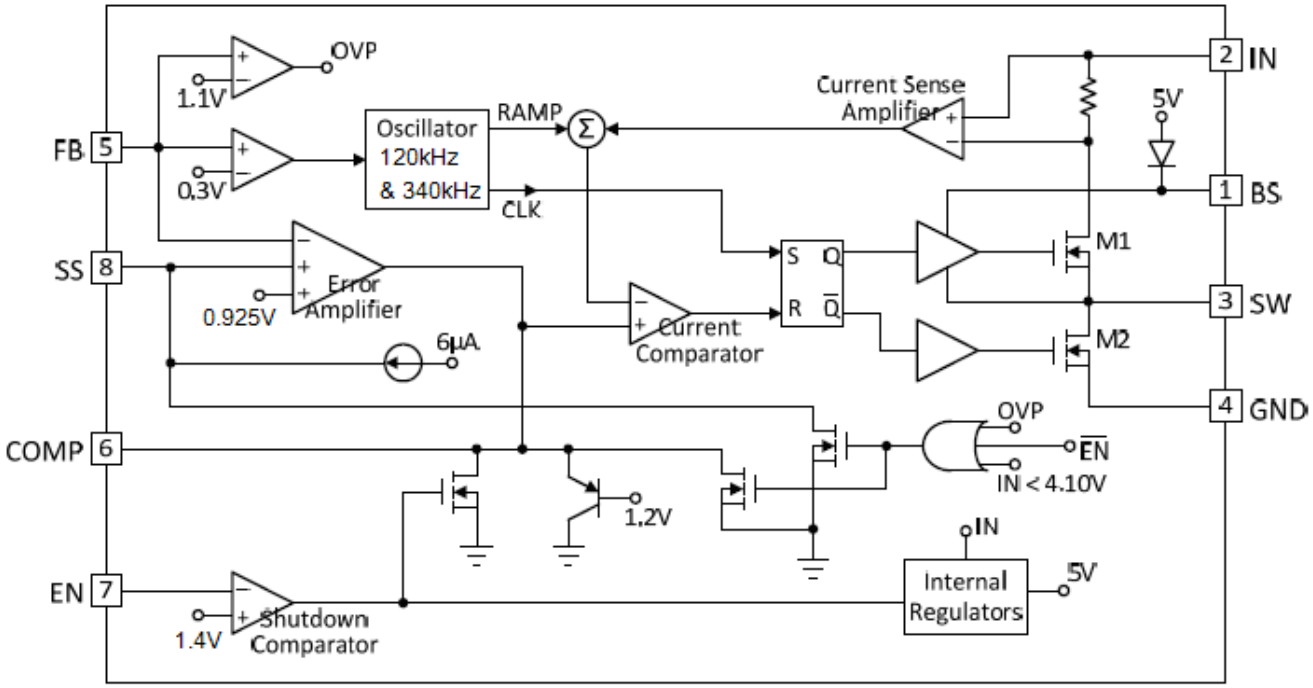
Pin Configurations



Pin Description

Number	Name	Description
1	BS	High-Side Gate Drive Boost Input. BS supplies the drive for the high-side MOS switch. Connect a 10nF or greater capacitor from SW to BS to power the switch.
2	IN	Power Input. Bypass to GND with a suitable large capacitor.
3	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.
4	GND	Ground.
5	FB	Feedback Input. Connect FB to the center point of the external resistor divider.
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop.
7	EN	Enable Input. When higher than 2.7V, this pin turns the IC on. When lower than 1.1V, this pin turns the IC off. Output voltage is discharged when the IC is off. This pin should not be left open. Recommend to put a 100KΩ pull up resistor to Vin for start up.
8	SS	Soft Start Control Input. SS controls the soft start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1μF capacitor sets the soft-start period to 15ms. To disable the soft-start feature, leave SS unconnected.

Function Block Diagram



Electrical Characteristics (V_{IN}=12V, V_{OUT}=3.3V, unless otherwise specified. Typical values are at T_A=25°C)

Parameters	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	4.5V to 23V V_{IN}	0.9	0.925	0.95	V
Feedback Overvoltage Threshold				1.1		V
High-Side Switch Current Limit		Mimunum Duty Cycle	3.8	4.5		A
COMP to Current Limit Transconductance	G_{CS}			5.2		A/V
Error Amp Transconductance		$\triangle I_{COMP}$ = +-10μA		900		μA/V
Error Amp DC Gain*				400		V/V
Switching Frequency	f_{SW}			340		KHz
Short Circuit Switching Frequency		V_{FB} = GND		100		KHz
Maximum Duty Cycle		V_{FB} = 0.8V		92		%
Minimum Duty Cycle			7.5			%
Enable Shutdown Threshold		V_{EN} Rising	1.1	1.4	2	V
Enable Shutdown Threshold Hysteresis				180		mV
EN Lockout Threshold Voltage			2.2	2.5	2.7	V
EN Lockout Threshold Hysteresis				150		mV
Standby Current		V_{EN} = GND, Shutdown		0.3	3	μA
Quiescent Current		V_{EN} = 3V, V_{FB} = 1.0V		1.3	1.5	mA
Input UVLO Threshold Rising	UVLO	V_{EN} = Rising	3.8	4.1	4.4	V
Input UVLO Threshold Hysteresis				150		mV
Soft Start Current		V_{SS} = 0V		6		μA
Soft Start Time		C_{SS} = 0.1μF		13		mS
Thermal Shutdown Temperature*		Hysteresis = 25℃		155		℃
High-Side Switch-On Resistance*				90		mΩ
Low-Side Switch-On Resistance*				70		mΩ
High-Side Switch Leakage		V_{EN} = 0V, V_{SW} = 0V		0.1	10	μA

* Guaranteed by design, not tested.

Applications Information

Overview

The iD8803 is a synchronous rectified, current-mode, step-down regulator. It regulates input voltages from 4.5V to 23V down to an output voltage as low as 0.925V, and supplies up to 3A of load current.

The iD8803 uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal transconductance error amplifier.

The voltage at the COMP pin is compared to the switch current measured internally to control the output voltage.

The converter uses internal N-Channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BS is needed to drive the high side gate. The boost capacitor is charged from the internal 5V rail when SW is low.

When the iD8803 FB pin exceeds 20% of the nominal regulation voltage of 0.925V, the over voltage comparator is tripped and the COMP pin and the SS pin are discharged to GND, forcing the high-side switch off.

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB pin. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$V_{FB} = V_{OUT} \times R2 / (R1 + R2)$

Where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Thus the output voltage is:

$V_{OUT} = V_{FB} \times (R1 + R2) / R2$

R2 can be as high as 100kΩ, but a typical value is 10kΩ.

Using the typical value for R2, R1 is determined by:

$R1 = 10.83 \times (V_{OUT} - 0.925)$ (kΩ)

Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$L = [V_{OUT} / (f_S \times \Delta I_L)] \times (1 - V_{OUT}/V_{IN})$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$I_{LP} = I_{LOAD} + [V_{OUT} / (2 \times f_S \times L)] \times (1 - V_{OUT}/V_{IN})$

Where I_{LOAD} is the load current.

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI requirements.

Optional Schottky Diode

During the transition between high-side switch and low-side switch, the body diode of the low-side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional Schottky diode of voltage 30V/1A current rating may be paralleled between the SW pin and GND pin to improve overall efficiency.

Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 10uF. The best choice is the ceramic type; however, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the VIN and GND pins of the IC, with the shortest traces possible. In the case of tantalum or electrolytic types, they can be further away if a small parallel 0.1uF ceramic capacitor is placed right next to the IC.

Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. In the case of ceramic output capacitors, ESR is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic capacitors. In the case of tantalum or electrolytic capacitors, the ripple is dominated by RESR multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.

For ceramic output capacitors, typically choose a capacitance of about 22uF. For tantalum or electrolytic capacitors, choose a capacitor with less than 50mΩ ESR.

Compensation Components

iD8803 employs current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP pin is the output of the internal transconductance error amplifier. A series capacitor and resistor combination sets a pole-zero combination to control the characteristics of the control system.

The DC gain of the voltage feedback loop is given by:

$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{EA} \times V_{FB}/V_{OUT}$

Where A_{EA} is the error amplifier voltage gain; G_{CS} is the current sense transconductance and R_{LOAD} is the load resistor value.

The system has two poles of importance. One is due to the compensation capacitor (C3) and the output resistor of the error amplifier, and the other is due to the output capacitor and the load resistor. These poles are located at:

$f_{P1} = G_{EA} / (2\pi \times C3 \times A_{EA})$

$f_{P2} = 1 / (2\pi \times C2 \times R_{LOAD})$

Where G_{EA} is the error amplifier transconductance.

The system has one zero of importance, due to the compensation capacitor (C3) and the compensation resistor (R3). This zero is located at:

$f_{Z1} = 1 / (2\pi \times C3 \times R3)$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$f_{ESR} = 1 / (2\pi \times C2 \times R_{ESR})$

In this case, a third pole set by the compensation capacitor (C6) and the compensation resistor (R3) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$f_{P3} = 1 / (2\pi \times C6 \times R3)$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system instability. A good rule of thumb is to set the crossover frequency below one-tenth of the switching frequency.

To optimize the compensation components, the following procedure can be used.

1. Choose the compensation resistor (R3) to set the desired crossover frequency.

Determine the R3 value by the following equation:

$R3 = [(2\pi \times C2 \times f_C) / (G_{EA} \times G_{CS})] \times (V_{OUT}/V_{FB})$

$< [(2\pi \times C2 \times 0.1 \times f_S) / (G_{EA} \times G_{CS})] \times (V_{OUT}/V_{FB})$

Where f_C is the desired crossover frequency which is typically below one tenth of the switching frequency.

2. Choose the compensation capacitor (C3) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero, f_{Z1}, below one-forth of the crossover frequency provides sufficient phase margin.

Determine the C3 value by the following equation:

$C3 > 4 / (2\pi \times R3 \times f_C)$

Where R3 is the compensation resistor.

3. Determine if the second compensation capacitor (C6) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency, or the following relationship is valid:

$1 / (2\pi \times C2 \times R_{ESR}) < f_S/2$

If this is the case, then add the second compensation capacitor (C6) to set the pole f_{P3} at the location of the ESR zero. Determine the C6 value by the equation:

$C6 = (C2 \times R_{ESR}) / R3$

External Bootstrap Diode

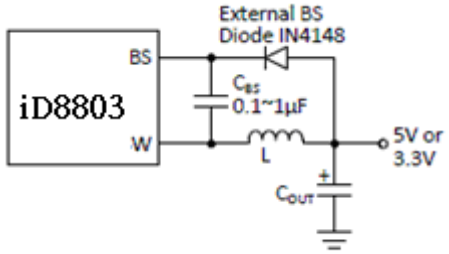
An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BS diode are:

● VOUT = 5V or 3.3V; and

● Duty cycle is high: $D = V_{OUT}/V_{IN} > 65\%$

In these cases, an external BS diode is recommended from the output of the voltage regulator to BS pin, as shown in Figure 1.

Figure 1: Add optional external bootstrap diode to enhance efficiency.



When $V_{IN} \leq 6V$, for the purpose of promote the efficiency, it can add an external Schottky diode between IN and BS pins, as shown in Figure 2.

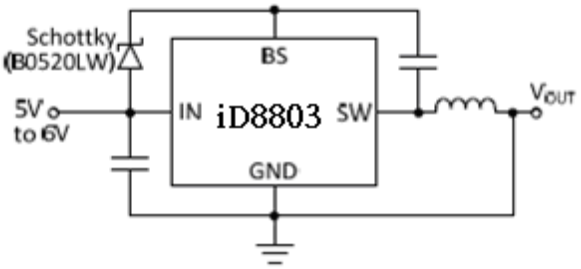
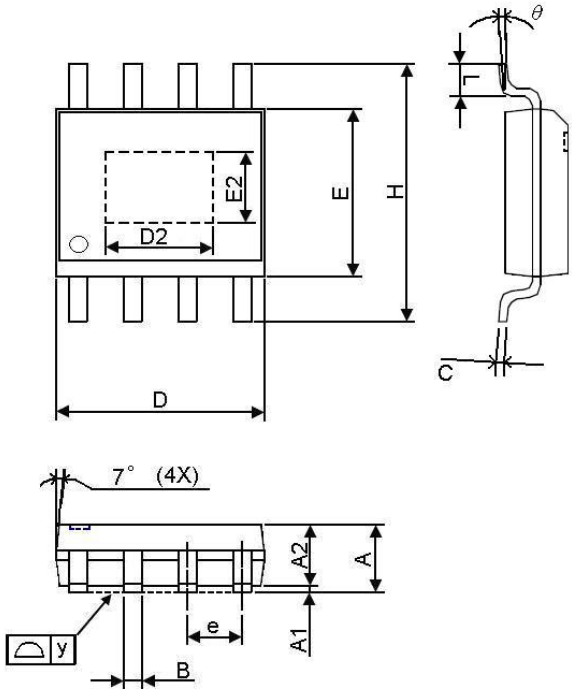


Figure 2: Add a Schottky diode to promote efficiency when $V_{IN} \leq 6V$.

Packaging

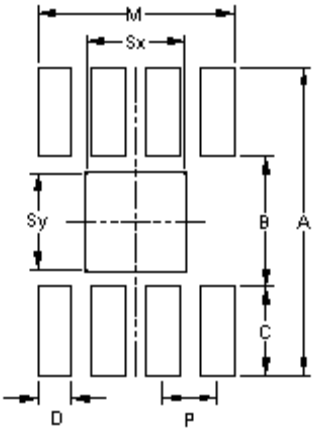
PSOP-8



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.40	1.50	1.65	0.055	0.059	0.064
A1	0.00	---	0.15	0.000	---	0.005
A2	1.3	1.4	1.5	0.051	0.055	0.059
B	0.33	---	0.51	0.013	---	0.020
C	0.19	---	0.25	0.007	---	0.010
D	4.70	---	5.10	0.185	---	0.200
D2	3.2	3.3	3.4	0.125	0.129	0.133
E	3.70	3.90	4.10	0.145	0.153	0.161
E2	2.3	2.4	2.5	0.090	0.094	0.098
e	---	1.27	---	---	0.050	---
H	5.80	---	6.20	0.228	---	0.244
L	0.40	---	1.27	0.016	---	0.050
y	---	---	0.10	---	---	0.004
θ	0°	---	8°	0°	---	8°

Footprints

PSOP-8



Package	Number of PIN	Footprint Dimension (mm)								Tolerance
		P	A	B	C	D	Sx	Sy	M	
PSOP-8	8	1.27	6.80	4.20	1.30	0.70	2.30 3.40	2.30 2.40	4.51	±0.10